**Chapter-8 (Practice Questions)**

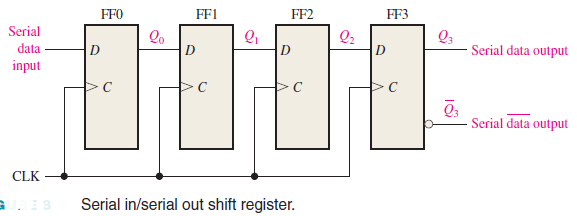
1. The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared.

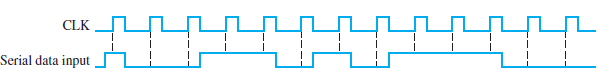
What is the state of the shift register after three clock pulses?

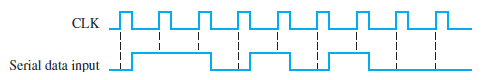
1. For the data input and clock in Figure 8–47, determine the states of each flip-flop in the shift

register of Figure and show the Q waveforms. Assume that the register contains all 1s

initially.

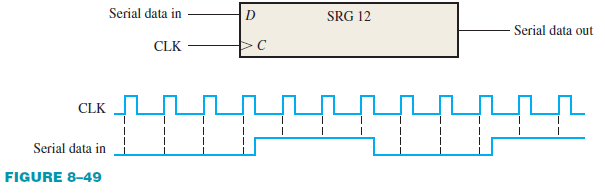


 (a)

(b)

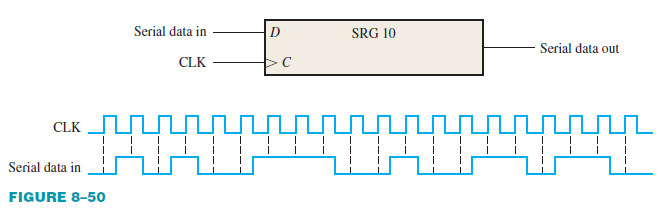
1. What is the state of the register in Figure 8–49 after each clock pulse if it starts in the

101001111000 state?



1. For the serial in/serial out shift register, determine the data-output waveform for the data-input

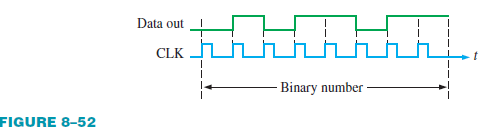
and clock waveforms in Figure 8–50. Assume that the register is initially cleared.



1. A leading-edge clocked serial in/serial out shift register has a data-output waveform as shown

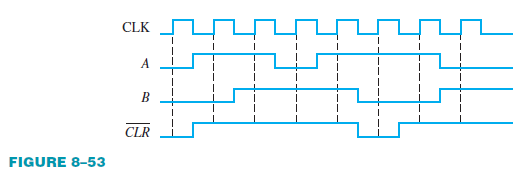
in Figure 8–52. What binary number is stored in the 8-bit register if the first data bit out (leftmost)

is the LSB?



1. Develop the Q0 through Q7 outputs for a 74HC164 shift register with the input waveforms

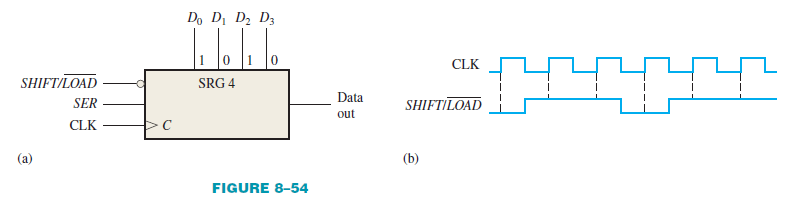
shown in Figure 8–53.



1. The shift register in Figure 8–54(a) has SHIFT/LOAD and CLK inputs as shown in part (b).

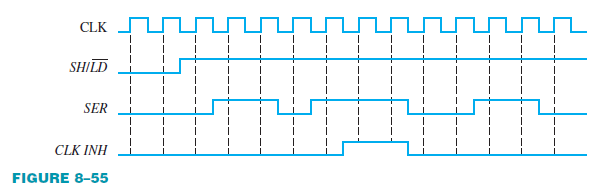
The serial data input (SER) is a 0. The parallel data inputs are D0 = 1, D1 = 0, D2 = 1, and

D3 = 0 as shown. Develop the data-output waveform in relation to the inputs.



1. The waveforms in Figure 8–55 are applied to a 74HC165 shift register. The parallel inputs are

all 0. Determine the Q7 waveform.



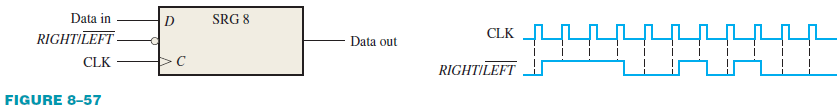
1. Solve Problem 8 if the parallel inputs are all 1.
2. For the 8-bit bidirectional register in Figure 8–57, determine the state of the register after each

clock pulse for the RIGHT/LEFT control waveform given. A HIGH on this input enables a shift

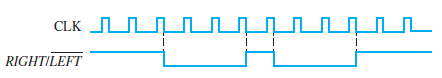
to the right, and a LOW enables a shift to the left. Assume that the register is initially storing

the decimal number seventy-six in binary, with the right-most position being the LSB. There is

a LOW on the data-input line.



1. Solve Problem 10 for the waveforms in Figure 8–58.

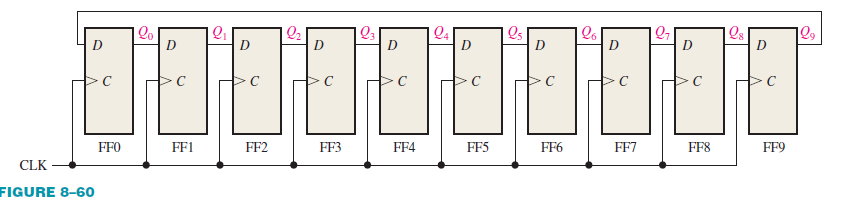


1. Draw the logic diagram for a modulus-18 Johnson counter. Show the timing diagram and write

the sequence in tabular form.

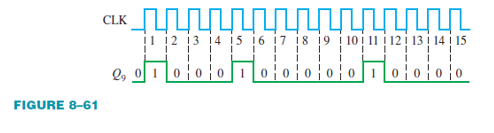
1. How many states are there in an 8-bit Johnson counter sequence?
2. Write the sequence of states for a 3-bit Johnson counter starting with 000.
3. For the ring counter in Figure 8–60, show the waveforms for each flip-flop output with respect

to the clock. Assume that FF0 is initially SET and that the rest are RESET. Show at least ten clock pulses.

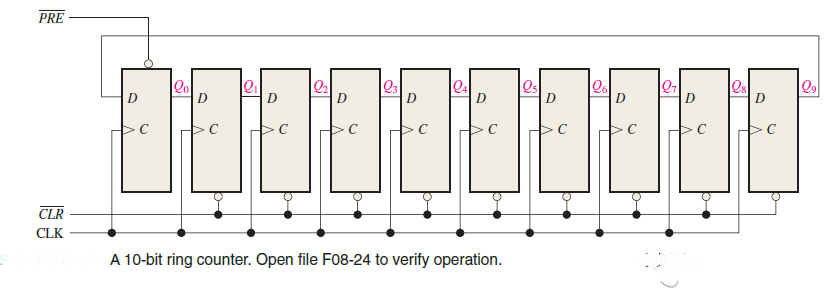


1. The waveform pattern in Figure 8–61 is required. Devise a ring counter, and indicate how it can

be preset to produce this waveform on its Q9 output. At CLK16 the pattern begins to repeat.



1. If a 10-bit ring counter similar to Figure 8–24 has the initial state 1010000000, determine

the waveform for each of the *Q* outputs. 

1. If a 10-bit ring counter has an initial state 0101001111, determine the waveform for

each *Q* output.